IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 2, 4, and 6-8, in accordance with the following:

1. (CURRENTLY AMENDED) A semiconductor memory comprising:

a plurality of sub memory units each having

a plurality of bit lines connected to memory cells~~, respectively~~, said bit lines corresponding to different data terminals with numbers, said sub memory units being arranged in a direction orthogonal to a wiring direction of said bit lines,

a plurality of sense amplifiers connected to said bit lines~~, respectively~~, and

a plurality of column switch circuits ~~for~~ connecting said bit lines to data bus lines, respectively;

a plurality of main memory units each ~~composed of~~comprising an even number of said sub memory units having different addresses from each other and comprising a defective sub memory unit;

a redundancy memory unit having at least one of said sub memory units, and being enabled when ~~a~~ said defective sub memory unit ~~of said sub memory units in said main memory units~~ is disabled; and

column switch areas formed in said main memory units~~, respectively~~, and having said column switch circuits arranged therein, wherein

every two of said column switch areas are formed in mirror symmetry in the wiring direction of said bit lines, and

for each of said data terminals, the data bus lines having a same logic are wired in said main memory units and said redundancy memory unit.

2. (CURRENTLY AMENDED) The semiconductor memory according to claim 1, wherein:

in each of said sub memory units, said column switch circuits are arranged in a row in the wiring direction of said bit lines, the column switch circuits corresponding to said data terminals, ~~respectively; and~~

in adjoining ones of said sub memory units in each of said main memory units, said column switch circuits are arranged ~~such that~~where sequences of the numbers of ~~their~~ said corresponding data terminals are opposite to each other.

3. (ORIGINAL) The semiconductor memory according to claim 2, wherein said data bus lines are wired along each row of said column switch circuits aligning in the direction orthogonal to the wiring direction of said bit lines.

4. (CURRENTLY AMENDED) The semiconductor memory according to claim 1, wherein

said column switch circuits each ~~have~~comprises:

a first transistor with ~~its~~ a first drain connected to any one of said data bus lines, and receiving a column selecting signal at ~~its~~ a first gate, the column selecting signal being selected in accordance with an address~~;~~, and

a second transistor with ~~its~~ a second gate connected to any one of said bit lines and ~~its~~ a second drain electrically connected to a source of said first transistor during a read operation.

5. (ORIGINAL) The semiconductor memory according to claim 1, wherein said data bus lines transfers read data read from said memory cells and write data to be written to said memory cells.

6. (CURRENTLY AMENDED) The semiconductor memory according to claim 5, wherein

said column switch circuits each ~~have~~comprises:

a first transistor comprising a first drain, a first gate, and a first source, ~~with~~where said ~~its~~ first drain is connected to any one of said data bus lines, and said first transistor ~~receiving~~ receives a column selecting signal at ~~its~~ said first gate, the column selecting signal being selected in accordance with an address~~;~~,

a second transistor comprising a second drain, a second gate, and a second source, where ~~with its~~said second gate is connected to said bit ~~line~~ lines and ~~its~~ said second source is connected to a source power supply~~;~~,

a third transistor comprising a third drain, a third gate, and a third source, where ~~with~~said ~~its~~ third drain is connected to ~~a~~ said first source ~~of said first transistor~~ and ~~its~~ said third source is connected to ~~a~~ said second drain ~~of said second transistor~~, and ~~receiving~~ receives a read control

signal at ~~its~~ said third gate, the read control signal turning to an activation level during a read operation~~;~~, and

a fourth transistor comprising a fourth drain, a fourth gate, and a fourth source, where said fourth ~~with its~~ drain is connected to said bit ~~line~~ lines and ~~its~~ said fourth source connected to said first source ~~of said first transistor~~, and receiving a write control signal at ~~its~~ said fourth gate, the write control signal turning to ~~an~~ said activation level during a write operation.

7. (CURRENTLY AMENDED) The semiconductor memory according to claim 1, further comprising:

a plurality of first column selecting lines ~~for~~ transmitting a plurality of bits of column selecting signals to said sub memory units~~, respectively~~, the plurality of column selecting signals being selected in accordance with said ~~address~~ addresses to ~~turn~~ turn-on said column switch circuits;

second column selecting lines formed in said sub memory units of said main memory units and of said redundancy memory unit~~, respectively~~, and connected to said column switch circuits;

a defect information memory part ~~for~~ storing defect information therein, the defect information indicating said defective sub memory unit; and

a redundancy switch part

connecting said first column selecting lines to said second column selecting lines, and

being switched according to contents stored in said defect information memory part corresponding to ~~disconnect~~ disconnecting said first column selecting lines from a defective second column selecting line of said defective sub memory unit, and to ~~connect~~ connecting said first column selecting lines to normal second column selecting lines, of said sub memory units in said main memory units and of said sub memory unit in said redundancy memory unit, the sub memory units in said main memory units operating normally.

8. (CURRENTLY AMENDED) The semiconductor memory according to claim 1, wherein:

each of said bit lines is either one of ~~each of~~ complementary bit line pairs~~;~~,

each of said data bus lines is either one of ~~each of~~ complementary data bus line pairs~~;~~,

said sense amplifiers are shared among said bit line pairs~~, respectively~~,~~;~~ and

each of said column switch areas ~~includes~~ comprises said column switch circuits

corresponding to said bit line pairs.